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Gate-tunable giant tunneling electroresistance in van der Waals ferroelectric tunneling junctions

Qinqin Wang [a,1], Ti Xie [a,1], Nicholas A. Blumenschein [b,1], Zhihao Song [a,1], Aubrey T. Hanbicki [b], Michael A. Susner [c], Benjamin S. Conner [d,e], Tony Low [f], Jian-Ping Wang [f], Adam L. Friedman [b], Cheng Gong [a,*]

[a] Department of Electrical and Computer Engineering and Quantum Technology Center, University of Maryland, College Park, MD 20742, USA
[b] Laboratory for Physical Sciences, College Park, MD 20740, USA
[c] Materials and Manufacturing Directorate, Air Force Research Laboratory, Wright-Patterson Air Force Base, OH 45433, USA
[d] Sensors Directorate, Air Force Research Laboratory, Wright-Patterson Air Force Base, OH 45433, USA
[e] National Research Council, Washington D.C. 20001, USA
[f] Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455, USA

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ABSTRACT

Ferroelectric tunneling junctions (FTJs) have attracted great interest due to their potential applications in non-volatile memories and neurosynaptic computing. In this work, high performance FTJs constructed with graphene and two-dimensional (2D) layered ferroelectric $CuInP_2S_6$ (CIPS) with out-of-plane polarization have been demonstrated. These van der Waals (vdW) heterostructure tunneling devices show tunneling electroresistance (TER) up to 10^7. Furthermore, the FTJs exhibit noticeable gate tunability, for which the on-state tunneling current can increase by 100% by applying a 50 V gate voltage through the conventional 260-nm-thick SiO_2 dielectric layer. Our demonstration of gate-tunable, giant tunneling electroresistance highlights its potential in energy-efficient non-volatile memories and computing-in-memory functions.

1. Introduction

Ferroelectric tunneling junctions (FTJs), a class of two-terminal devices consisting of a thin ferroelectric layer sandwiched between two electrodes, can exhibit strong tunneling electroresistance (TER) effect, thereby promising the next-generation energy-efficient non-volatile memories [1–6]. In FTJs, a thin ferroelectric layer serves as the electronic quantum tunneling layer and the electrical tunneling conductance can be modulated through the ferroelectric polarization reversal, which is the origin of the TER [2,7–9]. Traditionally, FTJs are mainly constructed based on three-dimensional (3D) ferroelectric materials, particularly the perovskite structure (ABO_3) family has been most extensively studied [10–13]. However, the depolarization field in conventional 3D ferroelectric materials impose a critical thickness, where the ferroelectric would fail if being scaled thinner, preventing the downscaling of switching voltages FTJs for low power operation [2,14–16]. Also, the unavoidable interfacial states in conventional 3D materials stacks compromise the TER, setting roadblocks for the realization of very high TER (typically for a perovskite oxide FTJ, the maximum TER was reported to be about 10^6) [1,17].

Recently, the emergent two-dimensional (2D) ferroelectric materials without surface dangling bonds show promise in breaking through the limitations of critical thickness in conventional 3D FTJs [18–23], enabling ultra-thin non-volatile memories and neurosynaptic computing micro-nano devices. To date, FTJs based on 2D ferroelectric materials (e.g., $CuInP_2S_6$ (CIPS), SnSe, etc.) have been demonstrated. Some of them exhibit high TER up to 10^7, which remains above 10^6 even after 5,000 cycles of writing/reading operations, showcasing the great potential for high endurance memory and computing applications [1]. Though many efforts have been devoted to this direction, challenges remain regarding device tunability and further enhancement of giant TER [4,24].

In this work, we fabricated FTJs based on the mechanically exfoliated 2D ferroelectric material CIPS on the standard SiO_2/Si substrate, and more than seven orders of TER between low- and high-resistance states are realized. Furthermore, we demonstrated that the on-state tunneling current can be effectively tuned by simply applying gate

* Corresponding author.
E-mail address: gongc@umd.edu (C. Gong).
[1] These authors contributed equally.

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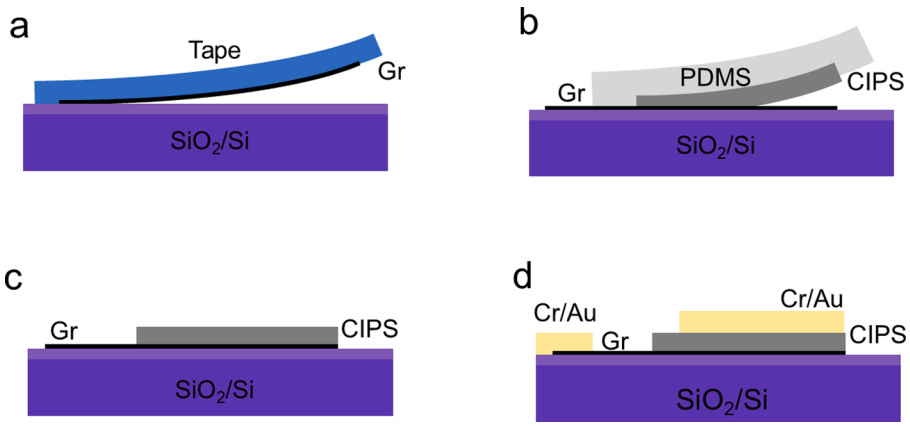

Fig. 1. (a-d) Schematic illustration of the fabrication process of FTJs. Ultrathin graphene flakes are mechanically exfoliated on 260-nm-thick-SiO_2/Si chips, followed by the mechanical exfoliation of ultrathin CIPS flakes by polydimethylsiloxane (PDMS) and being transferred onto the ultrathin graphene flakes under an optical microscope. Last, two 5-nm-Cr/50-nm-Au electrodes are defined by electron-beam lithography and deposited by thermal evaporation onto graphene and CIPS separately. When a small voltage is applied between these two electrodes, the electron tunneling can be expected through the ultrathin CIPS layer.

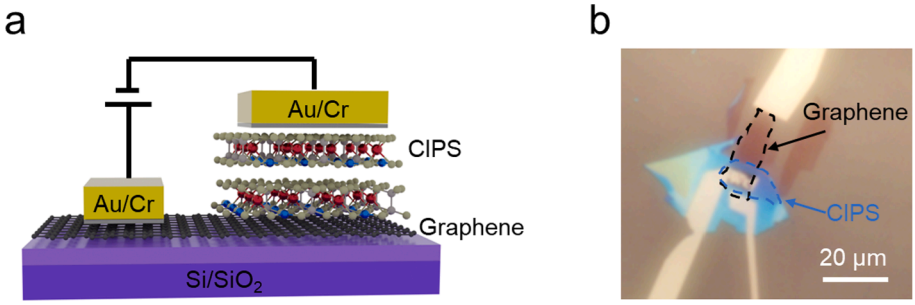

Fig. 2. (a) Schematic of the FTJ structure, consisting of a thin CIPS flake as the ferroelectrics and thin graphene and Cr/Au as two electrodes. (b) Optical image of the fabricated device. The regions surrounded by the blue and black dashed lines represent the top CIPS and the underneath few-layer graphene, respectively. Scale bar in b is 20 μm.

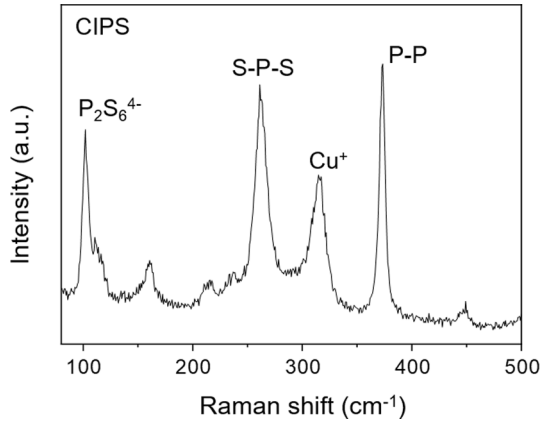

Fig. 3. Raman spectrum of a CIPS thin film at room temperature. The series of sharp Raman peaks are consistent with the previous experimental reports of high quality CIPS crystals [25–27], showcasing the excellent crystalline quality of our mechanically exfoliated CIPS flake. The crystal quality of the ferroelectric spacing layer will be critical for the large TER and sizable endurance.

voltages and the magnitude of the current increased monotonically as the voltage increased. Specifically, when applying a 50 V gate voltage, the on-state tunneling current can be doubled. The realization of giant TER with gate-tunable on-state current may open up practical avenues for enhanced functionality and configurability in next-generation non-volatile memories, logic devices, and logic-in-memory applications, including our envisioned band alignment ferroelectric-based random access memories (BAT-FE-RAM) and field effect transistors (BAT-FE-FET).

2. Device fabrication process

As shown in Fig. 1, the FTJs were fabricated through a layer-by-layer process. First, we mechanically exfoliated a few-layer graphene flake directly onto the 260-nm-thick-SiO_2/Si substrate. The ultrathin graphene flakes can be easily identified by their optical contrast under an optical microscope. Then, the thin CIPS film was exfoliated on polydimethylsiloxane (PDMS) and transferred onto the graphene flake using the all-dry viscoelastic stamping procedure under an optical microscope. The bilayer metallic electrodes (Cr/Au, 5/50 nm) were patterned using standard electron-beam lithography (EBL) and were deposited by thermal evaporation. In the whole flake exfoliation and transfer process, we did not notice the presence of bubbles in between vdW layers, indicating a good interfacial contact. Though we did not do intentional post annealing after the device fabrication, the unintentional heating associated with the thermal evaporation process can gently anneal the sample to strengthen the interfacial contact and release the unintentional strain. These are potential reasons for the excellent device performance (to be discussed later), even without subjecting our device to any post annealing treatments, a procedure that is commonly used in the field.

3. Device structure and spectroscopic characterization

Fig. 2(a) shows a schematic of the vdW FTJ device structure, where a thin CIPS flake serves as the tunneling layer, and the bottom and top electrodes are graphene and Cr, respectively. Fig. 2(b) shows a representative optical image of our fabricated tunneling device, and the area of the tunneling junction is about 40 μm^2. For this two-terminal device, the reading and writing will be through the same pair of electrodes. As will be discussed later, a pulse voltage will be applied to control the ferroelectric polarization. After the writing operation, we can

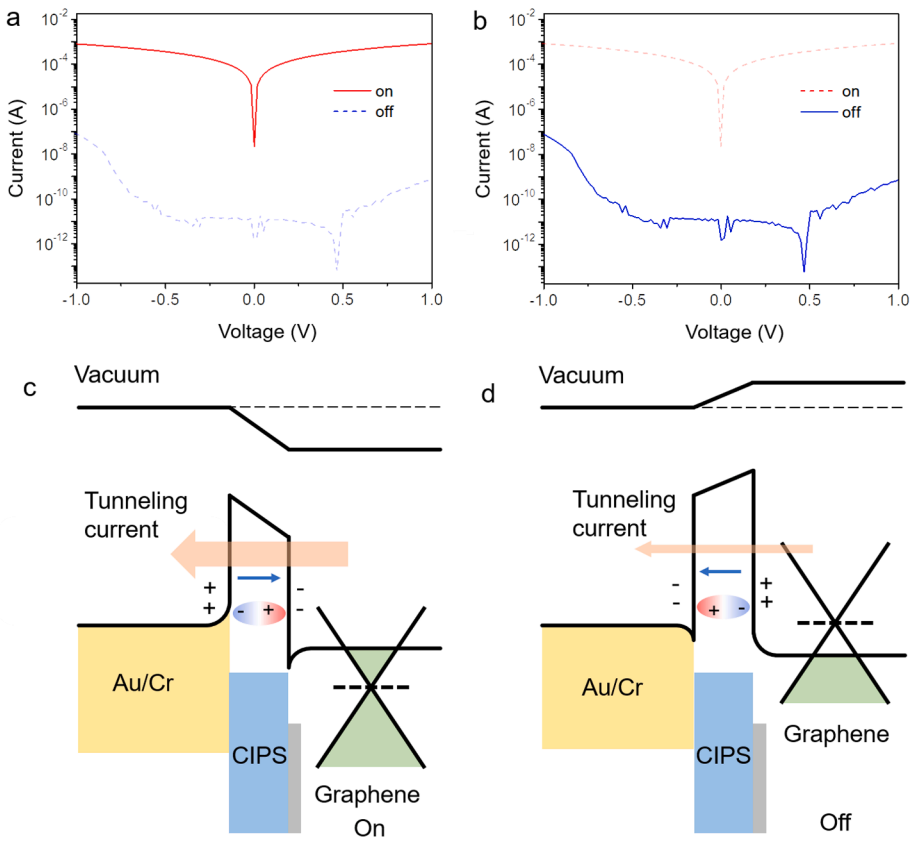

Fig. 4. Current-voltage characteristics and band diagrams of the FTJ. (a) Current-voltage characteristic of on-state. (b) Current-voltage characteristic of off-state. (c) Band diagrams for the on-state of the FTJ. (d) Band diagrams for the off-state of the FTJ. The built-in polarization fields in the CIPS are indicated by blue arrows, and the tunneling currents are indicated by light orange arrows.

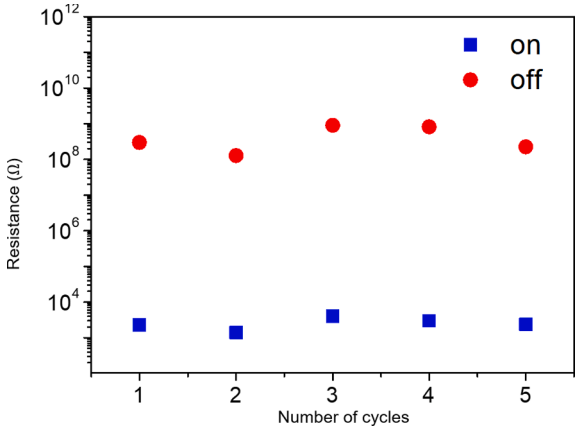

Fig. 5. Repetitive characterizations of the FTJ device. The writing and reading operations were repeated multiple times, and the clear contrast between ON and OFF states is highly reproducible.

subsequently sweep the voltage and measure the tunneling current.

Fig. 3 presents the Raman spectrum of an exfoliated CIPS thin film at room temperature with an excitation laser wavelength of 532 nm. The laser was focused on the sample via a 50 × objective with a numerical aperture of 0.5. One bandpass filter was used to clean up laser spectral noise, and three Bragg notch filters were used to suppress the Rayleigh line bandwidth down to ~ 8 cm^{-1}. The peak at around 100 cm^{-1} arises from the vibrations of anion ($P_2S_6^{4-}$), and the peak at 262 cm^{-1} is related to S-P-S vibrations. Cu^+ ions are responsible for the peak located at 316 cm^{-1}, and the peak at 373 cm^{-1} is caused by P-P stretching [25–27]. These well-defined Raman features agree well with the previous experimental reports based on high-quality as-synthesized bulk crystals of CIPS, indicating the high crystalline quality of our exfoliated CIPS flake. The high crystallinity with minimum density of defects will be critical for the high TER, sizable endurance and high threshold of voltages we can apply before dielectric breaks down or leakage current surges.

4. Devices performance

Here, we used pulse writing voltage with a period of 200 ms to flip the ferroelectric polarization of the tunneling devices, and after the writing operation and the withdrawal of the write voltage we recorded the tunneling current under a reading voltage of 0.4 V, or under a series of sweeping voltages, depending on specific measurement modes. To avoid the ferroelectric-paraelectric phase transition unintentionally caused by the Joule heating effect arising from the tunneling current, we used a low duty cycle (0.5%) to maintain the device temperature lower than the ferroelectric Curie temperature (T_C) of CIPS (~315 K) [28]. Before applying the writing voltages, we observed that the initial state of our fabricated FTJ (Fig. 2(b)) was in off-state with an extremely low tunneling current (~10^{-11} A) under 0.4 V reading voltage. To avoid breaking the device, we started from a relatively low pulse voltage (2 V) to try to flip the CIPS polarization, and the device remained in the off-state until the pulse voltage reached 3.4 V. After applying a pulse voltage of 3.4 V, the device switched to the on-state with a relatively high tunneling current (~10^{-4} A) under the same reading voltage (Fig. 4 (a)). By applying an opposite pulse voltage (−3.6 V), the FTJ device switched back to the off-state as shown in Fig. 4(b), which demonstrates a high TER up to seven orders of magnitude.

The giant modulation of the on/off-state tunneling currents arises

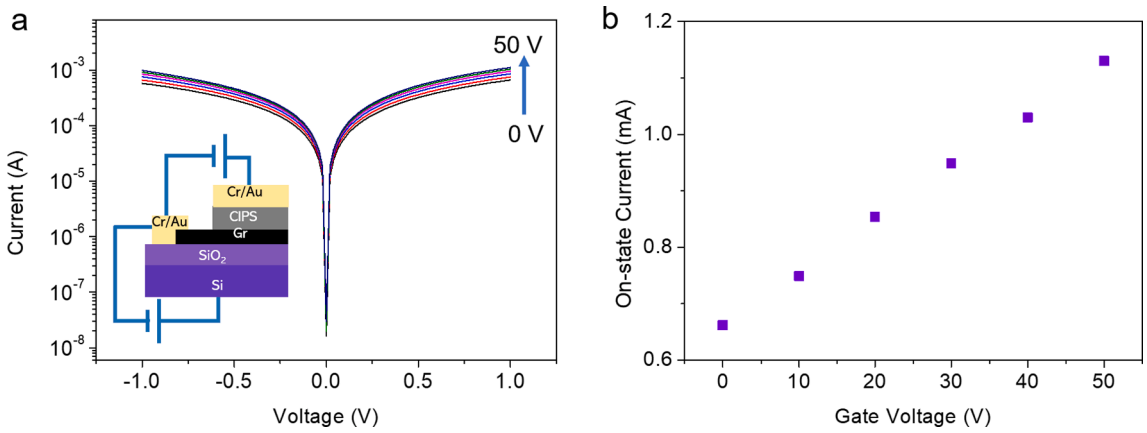

Fig. 6. (a) On-state current-voltage characteristics for FTJ under different gate voltages. Inset is the schematic of the device structure. 260-nm-thick SiO_2 served as the dielectric layer and the bottom Si (p++) served as the back-gate electrode. (b) On-state currents (with 1 V reading voltage) under different gate voltages. The magnitude of the tunneling current increases monotonically as the gate voltage increases.

from the following reasons: (1) the Fermi level of graphene can be effectively modulated by the CIPS layer of opposite polarizations, and (2) the tunnel barrier itself strongly depends on the built-in polarization electric field within the CIPS layer. Since the cold electron transmission probability depends exponentially on the barrier height, the difference between the Fermi level of graphene and the conduction band minimum of the CIPS barrier layer affects the tunneling current significantly.

With a positive writing voltage (3.4 V), the positive charge center (Cu^+) moves close to the graphene side and increases the electron concentration in graphene, causing the Fermi level of graphene to shift from relatively intrinsic to well above the Dirac point (n-doped). Therefore, the probability of electrons tunneling through the CIPS increases with the reduced height of the tunneling barrier, resulting in a larger tunneling current (on-state, Fig. 4(c)). Conversely, a negative writing voltage (−3.6 V) flips the polarization electric field in the opposite direction, which could reduce the electron concentration in graphene and shift the Fermi level below the Dirac point (p-doped). Correspondingly, the higher tunneling barrier between CIPS and graphene causes a remarkable decrease in the tunneling current (off-state, Fig. 4(d)).

Furthermore, as we continuously switched the positive and negative writing voltages, the on/off state of the FTJ device could be reliably and repeatedly controlled. In these operations, the TER could be maintained at $\sim 10^6$, as shown in Fig. 5. The off-state current we measured is on the order of 10^{-11} A (Fig. 4(b)), which is the equipment's measurable resolution of our Agilent 4155C semiconductor parameter analyzer. Per the data of the similar device reported in previous literature [1], the off-state current could be potentially on the order of 10^{-13} A or even lower. Considering our instrumental resolution in small current measurement, we reasonably expect that our true TER could be two orders of magnitude higher than the herein reported 10^7. We will leave this part of study to the future work.

Given the general tunability of 2D materials, it will be interesting to examine the tunability of the tunneling current in our FTJ devices, since if successful, it will be important for many device applications such as analog electronics and neurosynaptic computing [29–31]. Specifically, as illustrated in Fig. 2's device architecture, we used 260-nm-thick SiO_2 as the dielectric layer and the bottom Si (p++) served as the back-gate electrode. Fig. 6(a) depicts the on-state current-voltage characteristics of our FTJ with different gate voltages. The on-state currents increased with the increasing gate voltages at all the reading voltages (from −1 V to 1 V). Fig. 6(b) summarizes the on-state currents with a set 1 V reading voltage for different gate voltages. Without applying a gate voltage, the pristine on-state current is ~ 0.6 mA at 1 V reading voltage, which linearly increases with the increasing gate voltages. When the gate voltage increased to 50 V, the on-state current can achieve ~ 1.1 mA, which is around two folds of the pristine on-state current. The increased tunneling current is explained by the gate voltage raising the Fermi energy in graphene, leading to a decreased tunneling barrier height. The gate-tunable on-state current opens up new avenues to creating multiple intermediate states within the already large on/off window (10^7). We envision that the future work of engineering multiple states within the large on/off window may provide viable routes toward analogue electronics, neuromorphic computing, and computing in memory.

5. Conclusions

In this work, we constructed vdW heterostructure FTJs based on 2D ferroelectrics CIPS and 2D semimetal graphene, and the device exhibits a high TER up to 10^7. This high TER arises from the effective ferroelectric modulation of the chemical potentials in graphene and the tunneling barrier height. Remarkably, the tunneling current can be further tuned by simply applying a gate voltage to control the energy levels in graphene, leading to a further enhancement and fine tuning of the TER. Based on these results, we envision that the TER can be further enhanced by employing high-K dielectrics to electrostatically control graphene. Our gate-tunable vdW FTJs with giant TER opens up new platforms for high-performance non-volatile memories, logic devices, and logic-in-memory applications, including our envisioned BAT-FE-RAM and BAT-FE-FET.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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